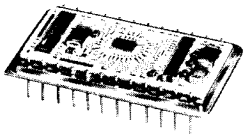
DDC
ILC DATA DEVICE CORPORATION

MONOBRID® ADH-030 II

12 BIT 35 NSEC HYBRID D/A CONVERTER
High Reliability; One Monolithic Active Component



FEATURES

- *FAST: 35 NSEC SETTLING*
- *HIGH RELIABILITY: 3,000,000 HOUR MTBF*
- *LOW GLITCH: 50 MV · NSEC*
- *–55° to +125°C OPERATING TEMPERATURE*
- *HERMETICALLY SEALED 24 DDIP PACKAGE*

DESCRIPTION

The Monobrid ADH-030 II is a 12 bit 35 nanosecond hybrid D/A converter packaged in a hermetically sealed 24 DDIP. It pin for pin replaces an earlier multiple component design with a single monolithic integrated circuit. Thin film resistors and decoupling capacitors complete the (monolithic-hybrid) Monobrid. Featuring 3,000,000 hour MTBF, 50 mV • nsec glitch, and -55°C to +125°C operating temperature range, the Monobrid ADH-030 II is offered with MIL-STD-883B screening.

APPLICATIONS

With its small size, wide operating temperature range and hermetically sealed package, the Monobrid ADH-030 II is ideal for the most demanding military and industrial requirements. Its high speed and low glitch are well suited for numerous CRT display applications, including TV and radar video reconstruction, and X-Y deflection positioning. Additional applications include digitally controlled frequency agile oscillators and high speed A/D converters.

Note: Monobrid® is a registered trademark of ILC Data Device Corp.

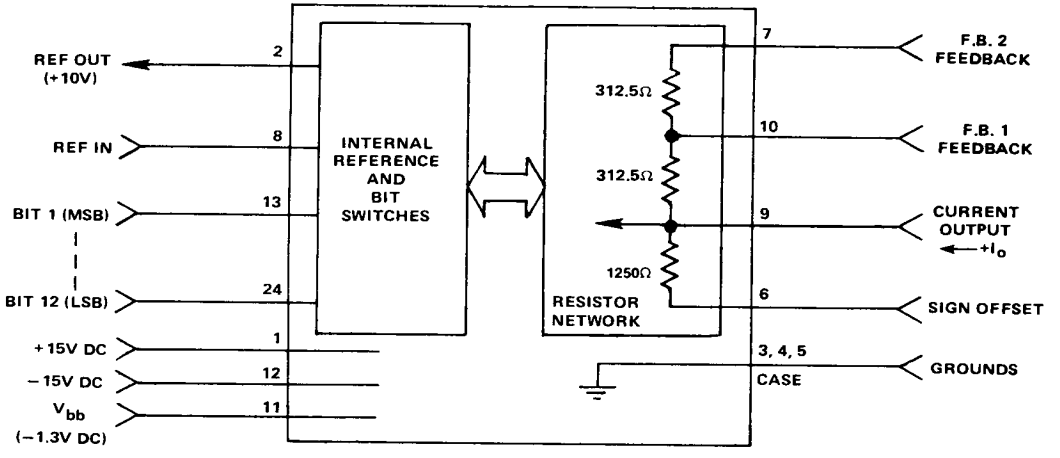


FIGURE 1. ADH-030 II BLOCK DIAGRAM

TABLE 1. ADH-030 II SPECIFICATIONS

Typical values at 25°C and at nominal power supply voltages unless otherwise noted.

PARAMETER	UNIT	VALUE	
		10 BIT LIN	12 BIT LIN
RESOLUTION	Bits	12	12
ACCURACY			
Linearity Error (Max)	% F.S. Range	±0.05	±0.0125
Linearity Tempco*	ppm/°C	±5	±5
Gain Accuracy	% F.S. Range	±0.1	±0.1
Gain Tempco*	ppm/°C	50	25
Zero Offset			
Unipolar Offset (Max)	μA	4	1
Bipolar Offset (Max)	μA	8	4
Offset Tempco	ppm/°C	20	10
Monotonic to	bits	10	12
DYNAMIC CHARACTERISTICS			
Update Rate	MHz	50 min	
Settling Time to 0.01% of Final Value			
For F.S. Input Change	ns	35 typ;, 50 max	
For 1 LSB Change (From 01..11 to 10..00)	ns	20 typ	
Internal Skewing Time	ps	400 typ; 800 max	
Output Time Constant	ns	1.3 typ into 100Ω load	
Glitch Energy	LSB·nsec	200	
	mV·nsec	50 into 100Ω	
DIGITAL INPUT (VALUES GIVEN FOR V_{bb} = −1.30V DC)			
Input Coding		Positive logic. Complementary Binary gives unipolar ouput. Complementary Offset Binary or Complementary Two's Complement (if MBS is provided) give bipolar output.	
		Logic "1"	Logic "0"
Digital Voltage Level	V	−0.81 to −0.96	−1.65 to −1.85
Max Voltage Without Damage	V	0	−6
Current Loading	μA	100 max	1 max
REFERENCE AND SIGN OFFSET		10 BIT LIN	12 BIT LIN
Internal +10.000V Reference Accuracy	% of Ref	±0.2 max	±0.1 max
Max Current Output**	mA	15 max	
External Ref. Requirements (Optional)			
Voltage Range	V	+10 ± 10%	
Current Requirements			
For Ref Input	mA	4.0 typ; 4.4 max	
For Sign Offset	mA	8.0 typ; 8.8 max	
Ref. Input Impedance	KΩ	2.5 ± 1%	
Sign Offset Impedance	KΩ	1.25 ± 1%	
OUTPUT (CURRENT TYPE)			
Unipolar Current	mA	0 to −16	
Bipolar Current	mA	±8	
Compliance	V	−0.5 to +5.0	
Voltage Output Ranges With External Amplifier	V	Full accuracy; 0 to 5 0 to 2.5, ±5, ±2.5, ±1.25 Reduced Accuracy: 0 to 10	
Output Capacitance	pF	20 typ	

TABLE 1. ADH-030 II SPECIFICATIONS (Cont'd)

PARAMETER	UNIT	VALUE		
POWER SUPPLIES				
Voltage	V	+15	−15	−1.3 (V_{bb})
Regulation for Full Accuracy	%	±2	±2	±3
Absolute Max Limit	V	+18	−18	−4
Current Typ	mA	30	57	0.5
Max	mA	35	60	2
TEMPERATURE RANGE (CASE)				
Operating				
−1 Option	°C	−55 to +125		
−3 Option	°C	0 to +70		
Storage	°C	−55 to +125		
THERMAL IMPEDANCE***				
Junction to Air, θ_{JA}	°C/Watt	20 max		
Junction to Case, θ_{JC}	°C/Watt	2 max		
PHYSICAL				
Package		24 Pin, Double DIP		
Size	inches	1.4 x 0.8 x 0.2		
	(mm)	(36 x 20.3 x 5.1)		
Weight	oz	0.4 (11.3 g) typ		

*Lower Tempco values are available — consult factory.
**If reference is used by external circuits only, load must be 5 mA minimum.
***Max junction temperature is 150°C.
Heat passes through header (case bottom).

TECHNICAL INFORMATION

INTRODUCTION

The ADH-030 II generates analog output currents which are digitally controlled, binary weighted, discrete fractions of a reference voltage. The reference voltage is fixed so that the output current has a single value for each digital input code. A reference is generated internally, as indicated in the block diagram Figure 1, but a properly regulated external reference voltage may be substituted. The analog output is controlled by a ladder network of thin film precision resistors, controlled by bipolar transistor switches turned on and off in accordance with the digital input code.

Figure 2 is an internal schematic for the ADH-030 II showing the 8 mA current generators, the R-2R ladder network, and the external connections. Feedback resistors are provided to assist in converting the current output into a voltage output with an external amplifier, as discussed below. The sign offset (pin 6) is used for bipolar operation, as discussed below. Note that the current direction is defined as positive for currents entering the output, pin 9.

The ADH-030 II accepts complementary binary or complementary offset binary input coding. The MECL/ECL input logic requirements are detailed in the specifications table. Figure 3 shows the current outputs obtained for various bit weights. The values for Full Scale (F.S.) and 1 LSB are as follows:

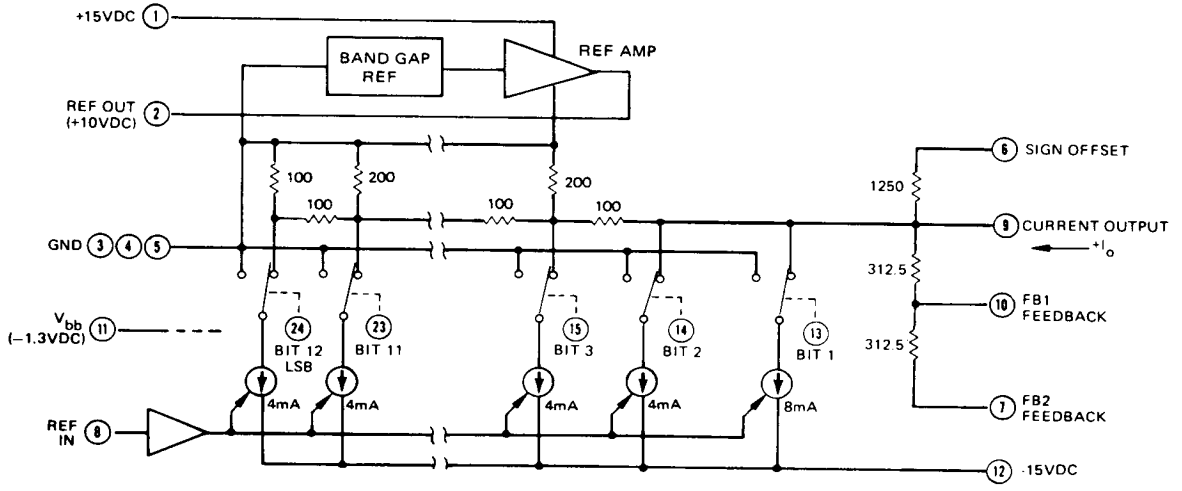


FIGURE 2. ADH-030II INTERNAL SCHEMATIC

ANALOG OUTPUT CURRENT*		DIGITAL BIT INPUTS											
UNIPOLAR COMPLEMENTARY BINARY	BIPOLAR COMPLEMENTARY OFFSET BINARY	MSB 1	2	3	4	5	6	7	8	9	10	11	LSB 12
+F.S. −1 LSB	+F.S. −1 LSB	0	0	0	0	0	0	0	0	0	0	0	0
+¾ F.S.	+½ F.S.	0	0	1	1	1	1	1	1	1	1	1	1
+½ F.S. +1 LSB	+1 LSB	0	1	1	1	1	1	1	1	1	1	1	0
+½ F.S.	0	0	1	1	1	1	1	1	1	1	1	1	1
+½ F.S. −1 LSB	−1 LSB	1	0	0	0	0	0	0	0	0	0	0	0
¼ F.S.	−½ F.S.	1	0	1	1	1	1	1	1	1	1	1	1
+1 LSB	−F.S. +1 LSB	1	1	1	1	1	1	1	1	1	1	1	0
0	−F.S.	1	1	1	1	1	1	1	1	1	1	1	1

*Current direction defined as positive for currents entering the output.

FIGURE 3. BIT WEIGHT TABLE

RANGE	FULL SCALE	1 LSB
±8 mA	8.00000 mA	0.00391 mA
0 to −16 mA	16.00000 mA	0.00391 mA
±1.25*	1.25000V	0.00061V
±2.5*	2.50000V	0.00122V
±5V*	5.00000V	0.00244V
0 to +2.5V*	2.50000V	0.00061V
0 to +5V*	5.00000V	0.00122V
0 to +10V*	10.00000V	0.00244V

*With external output amplifier

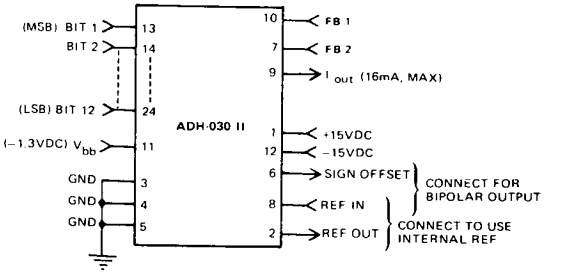


FIGURE 4. INPUT/OUTPUT CONNECTIONS FOR NORMAL OPERATION

NORMAL OPERATION

1. Normal Operation/Current Type Output

The input/output connections for normal operation of the ADH-030 II are shown in Figure 4.

For unipolar current output, the maximum output voltage is limited by the — 16 mA current capability to

$$V_{max} = -0.016R, \frac{1}{R} = \frac{1}{200} + \frac{1}{RL}$$

where RL is the load resistance and 200Ω is the resistance of the ladder network. The compliance limits V_{max} to −0.5V, so the load resistance should be 37Ω or less.

For bipolar operation the sign offset must be connected to the REF IN. The 1250Ω sign offset resistor (see Figure 2) is in parallel with the 200Ω ladder network, reducing the internal impedance at the output to 172.4Ω. The maximum output voltage is limited by the ±8mA current to

$$V_{max} = \pm 0.008R, \frac{1}{R} = \frac{1}{172.4} + \frac{1}{RL}$$

Since the compliance is −.5 V to +5 V, the load resistance should be 98Ω or less.

2. Normal Operation/Voltage Type Output

The ADH-030 II provides up to −0.5V to +5.0V compliance, so external circuitry must be added if a larger voltage swing is required.

Figure 5 shows an optional circuit for converting the ADH-030 II current output to a voltage type output. The voltage range is determined by connections to the feedback pins FB1 and FB2 on the ADH-030 II. Adding a jumper between pins 6 and 8 provides offset for bipolar operation. The following table shows jumper and feedback connections for all voltage ranges.

3. Trimmed Operation

Without external trimming, the output accuracy of the ADH-030 II is affected by the gain accuracy and zero offset error listed in the specifications. Using external trim resistors the gain and offset errors can be trimmed to zero so that the overall accuracy is equal to the linearity.

Figure 6 shows input/output connections for trimmed operation. The zero offset adjustment range is approximately ±20 LSB. The gain adjustment is provided by a resistor which replaces the direct connection between REF OUT and REF IN. The gain adjustment range is 3% in the direction of *decrease* only. To provide for adjustments in the opposite direction, the gain must be offset. This can be accomplished in conjunction with the voltage output circuit of Figure 5 by inserting a 10 or 5Ω resistor in the feedback path, as indicated at pins 7 and 10 in Figure 6.

VOLTAGE RANGE	JUMPER CONNECTIONS	FEEDBACK CONNECTIONS
±1.25V	Sign to Ref In, FB2 to current out	FB1
±2.5V	Sign to Ref In	FB1
±5V	Sign to Ref In	FB2
0 to +2.5V	FB2 to current out	FB1
0 to +5V	None	FB1
Reduced Accuracy: 0 to +10V	None	FB2

Note that on the 0 to +10 voltage range, the overall accuracy of the ADH-030 II is reduced to 0.2% F.S. range for all linearity grades.

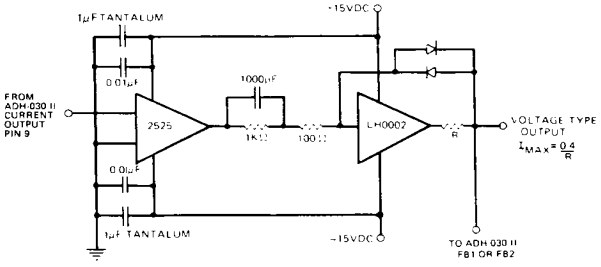


FIGURE 5. EXTERNAL CIRCUIT FOR VOLTAGE TYPE OUTPUT

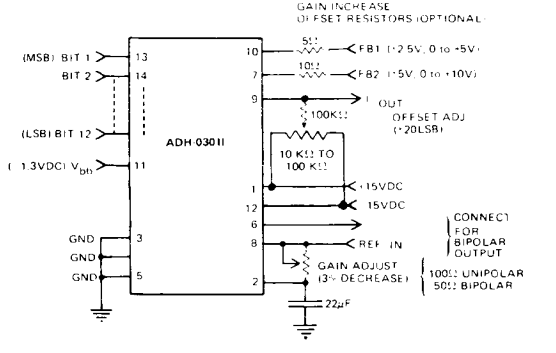


FIGURE 6. INPUT/OUTPUT CONNECTIONS FOR TRIMMED OPERATION

LINEARITY AND ACCURACY TESTS

Accuracy may be tested as follows: Connect pins 2, 6, and 8 together. Install the voltage output circuit of Figure 5 with direct feedback to FB2 (±5.0V output). The table in Figure 3 can be used to calculate the appropriate bit weights. A voltmeter with ±0.001V accuracy is required to measure the output. Unless a computer program is available to analyze the data, the most convenient test procedure is as follows:

(1) Measure the offset at the code 4 zero voltage.

(2) Install offset trim resistors and trim the offset error to zero. Determine the gain by measuring the output at both the +F.S. −1 LSB and −F.S. The gain is the sum of the magnitudes of the two end point voltages divided by 2 F.S. −1 LSB = 9.99756V.

(3) Install gain trim resistors and trim the gain to unity. Measure the output at all other codes to determine the linearity error.

The measured errors shall all be within the limits listed in the specifications table.

DYNAMIC CHARACTERISTICS

Skew is the difference in delay between individual bit transitions. When data changes, internal or external differences in delays between 0-1 and 1-0 transitions can cause the output to swing to intermediate states. For instance, if the input changes from 100 . . . 0 to 011 . . . 1 and the MSB changes before the lower order bits change, the output will swing to an intermediate state of 00 . . . 0. Internal skew is very low (400 ps typical) in the ADH-030 II because current mode switching is utilized. The MECL/ECL logic required by the digital input has inherently low skew properties, but to eliminate the last nanoseconds of skew it is necessary to clock the input with a register and match external circuit delays and line length differences. To maintain minimum skew with variations in temperature and power supplies, it is recommended that ADH-030 II pin 11 be connected to the V_{bb} output pin of an ECL logic circuit such as the MC10115.

Glitch energy is only 50 mV · nsec typ. Figure 7 shows glitch shape at major carry from 01 . . . 11 to 10 . . . 00 when the output is terminated by a 5 MHz filter and a 100 ohm resistor.

Settling time may be tested using the circuit shown in Figure 8. For a maximum output swing between —0.5V and +0.5V, the output will settle to 0.01% of final value within 50 ns (35 ns typical). For a swing of 1 LSB, the settling time depends on the skew and resulting glitch. For a 1 LSB change at major carry from 01 . . . 11 to 10 . . . 00, the settling time is 20 ns typical.

Ringing caused by long lead lengths or unterminated transmission line effects in the bit drives may lead to increased settling time or cause oscillation. If the lead length can not be shortened, the effect may be reduced or eliminated by placing RF beads on every other digital input lead.

REFERENCE

The ADH-030 II has an internal reference supply and is factory calibrated with this supply. Fixed external references of +10VDC ±10% can be accommodated and the output current will be linearity proportional to the reference voltage over this range.

RELIABILITY

The use of a single monolithic I.C. and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

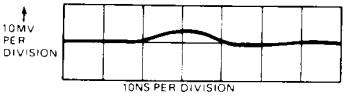


FIGURE 7. TYPICAL GLITCH SHAPE FOR 1 LSB CHANGE AT MAJOR CARRY (INTO 100Ω LOAD)

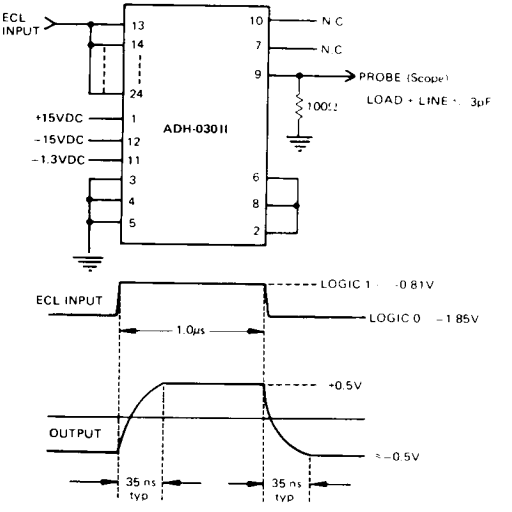


FIGURE 8. SETTLING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

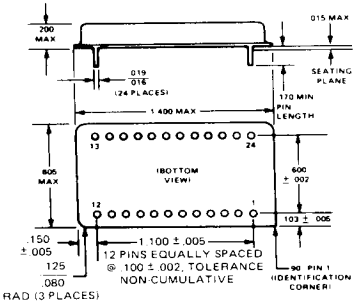
B

PIN CONNECTION TABLE

PIN No.	FUNCTION	PIN No.	FUNCTION
1	+15VDC	13	Bit 1 (MSB)
2	Ref. Out	14	Bit 2
3	Gnd*	15	Bit 3
4	Gnd*	16	Bit 4
5	Gnd*	17	Bit 5
6	Sign Offset	18	Bit 6
7	Feedback 2	19	Bit 7
8	Ref. In	20	Bit 8
9	Output	21	Bit 9
10	Feedback 1	22	Bit 10
11	$-1.3VDC = V_{bb}$	23	Bit 11
12	−15VDC	24	Bit 12 (LSB)

*All grounds are tied to the case.

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply at seating plane
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

ORDERING INFORMATION

ADH-030 II–12–1–883B

Reliability Grade:
- 883B = Fully compliant with MIL-STD-883
- B = Screened to MIL-STD-883 but without QCI testing.
- Blank = Standard DDC procedures.

Operating Temperature Range (Case)
- 1 = −55°C to +125°C
- 3 = 0°C to +70°C

Linearity:
- 10 = ±.05%
- 12 = ±.0125%

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